

FIG. 1 is a schematic diagram of a semiconductor device layout. The diagram shows a central horizontal strip (100) with a hatched pattern, flanked by vertical strips (200) with a dotted pattern. The central strip is divided into sections (14, 15, 16) by horizontal lines (30). The vertical strips are divided into sections (40, 60) by horizontal lines (30). The entire structure is enclosed in a dashed box (1000). A coordinate system (X, Y) is shown in the top right corner. Labels B0, B1, and B2 indicate specific regions of the device.

FIG. 2

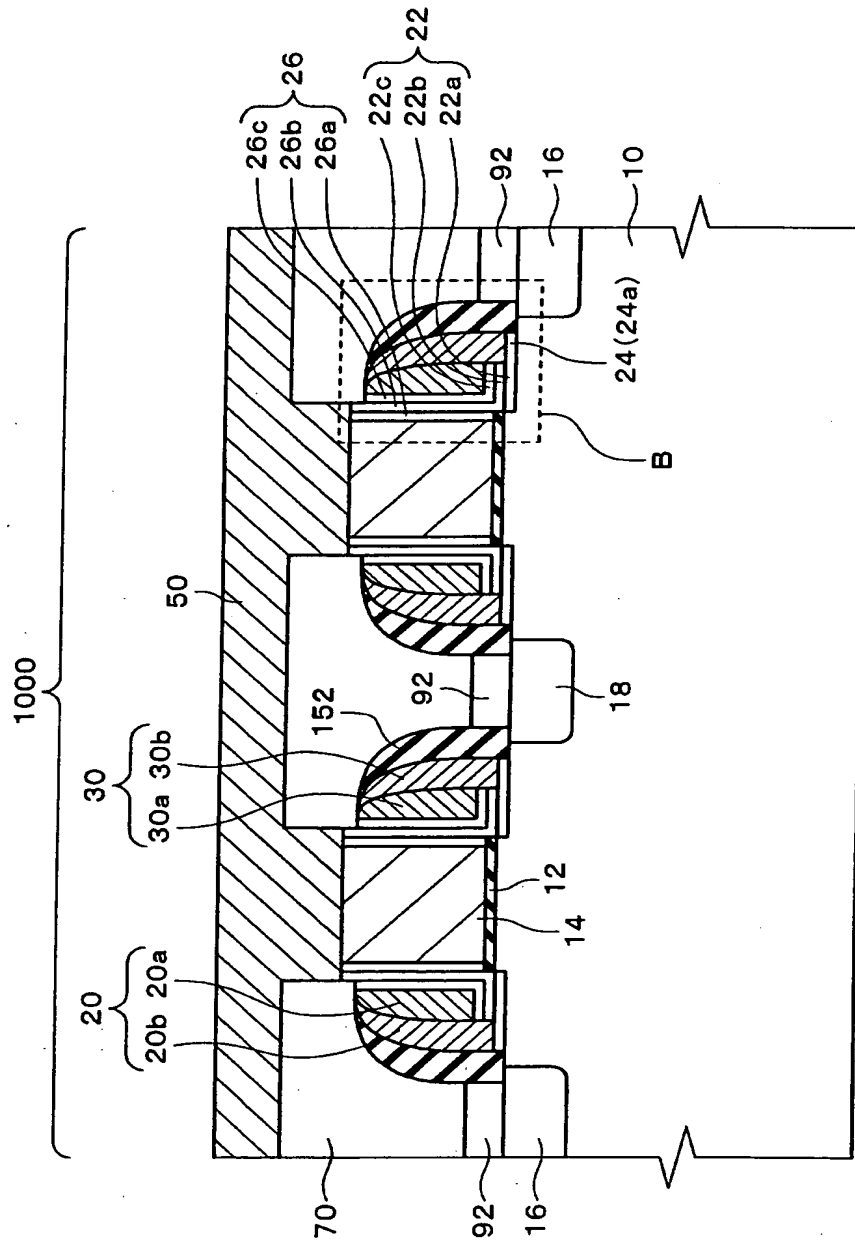


FIG. 3

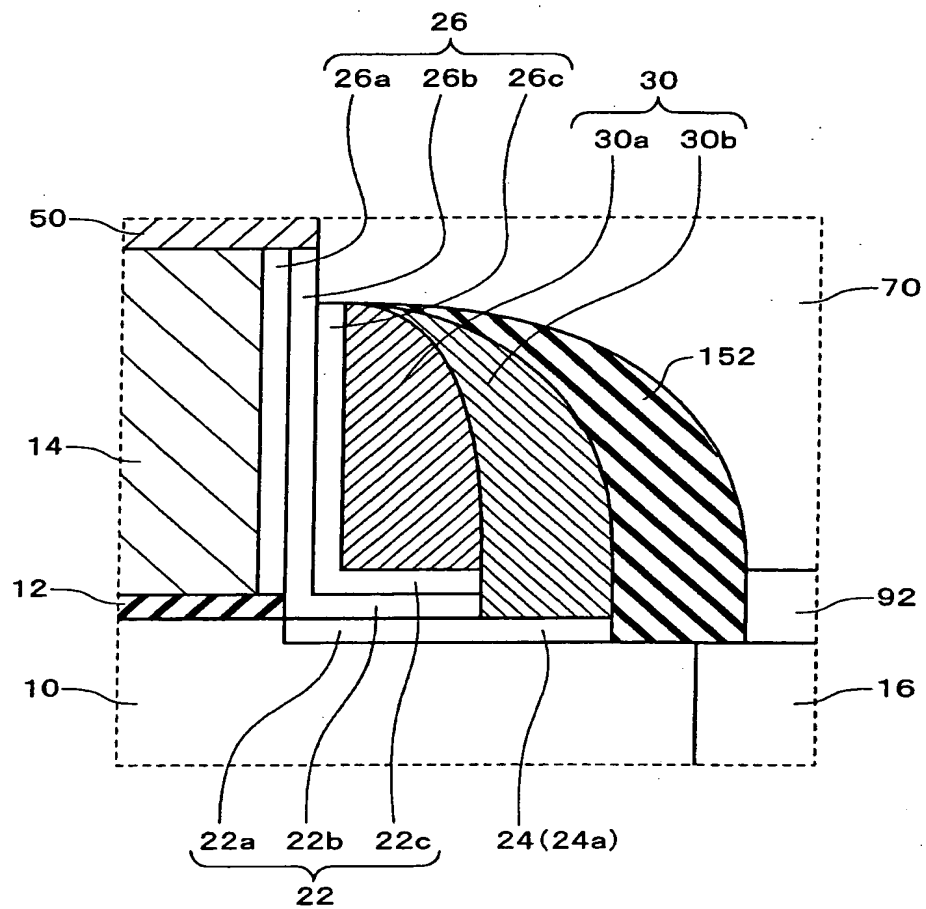


FIG. 4

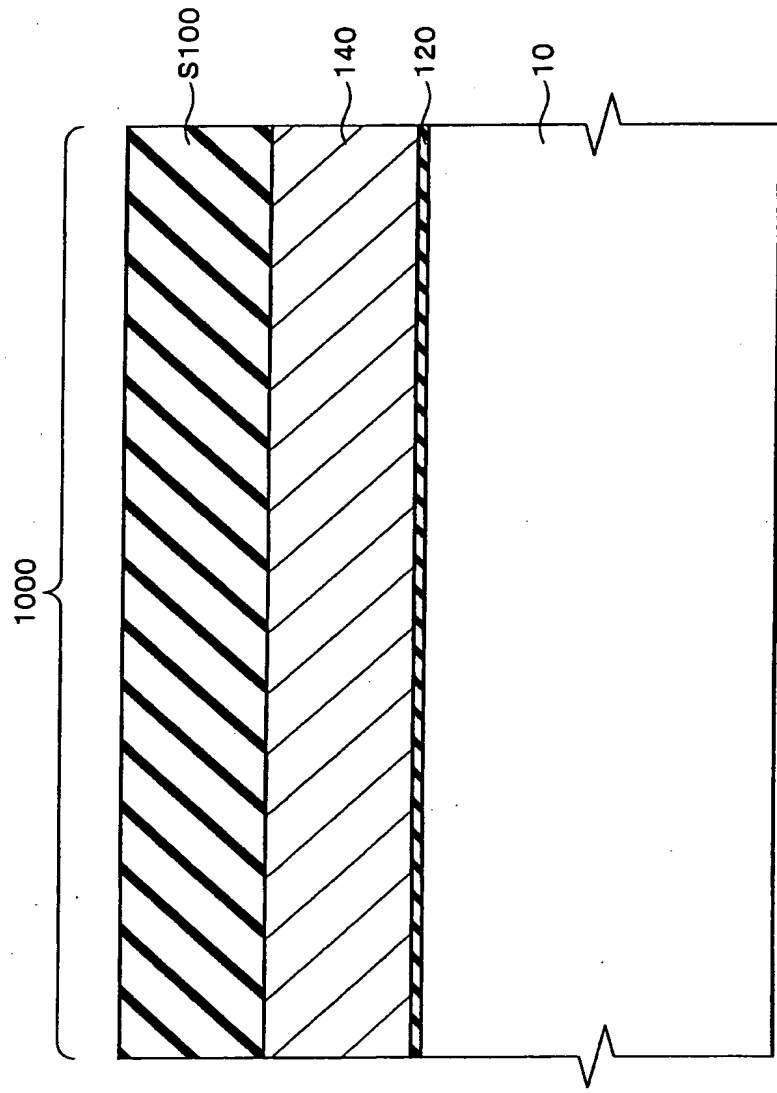


FIG. 5

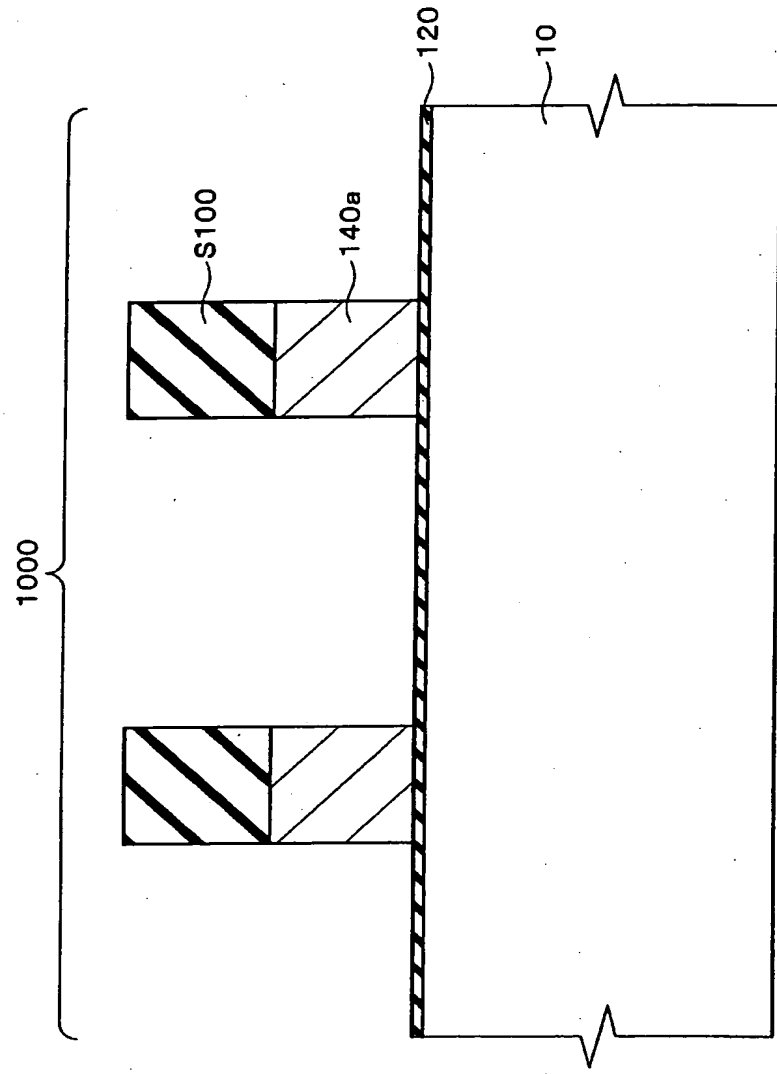


FIG. 6

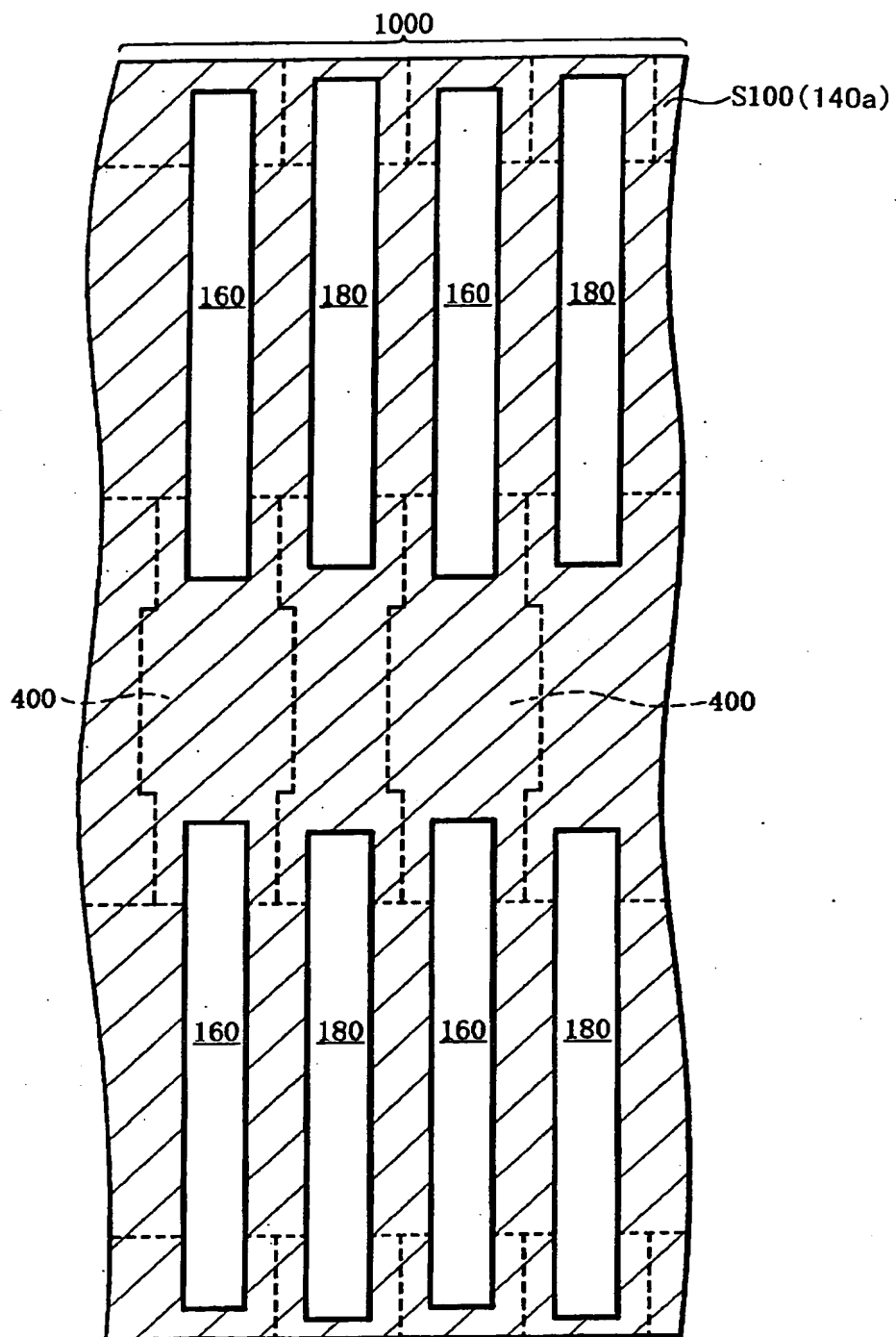


FIG. 7

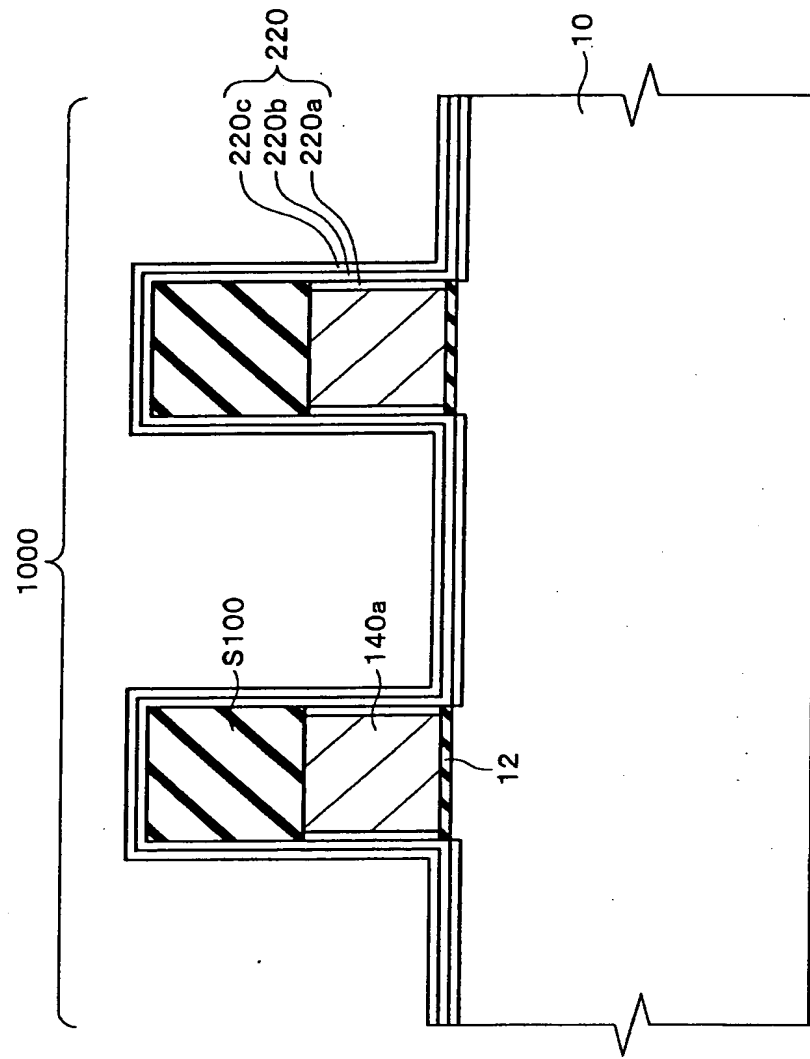


FIG. 8

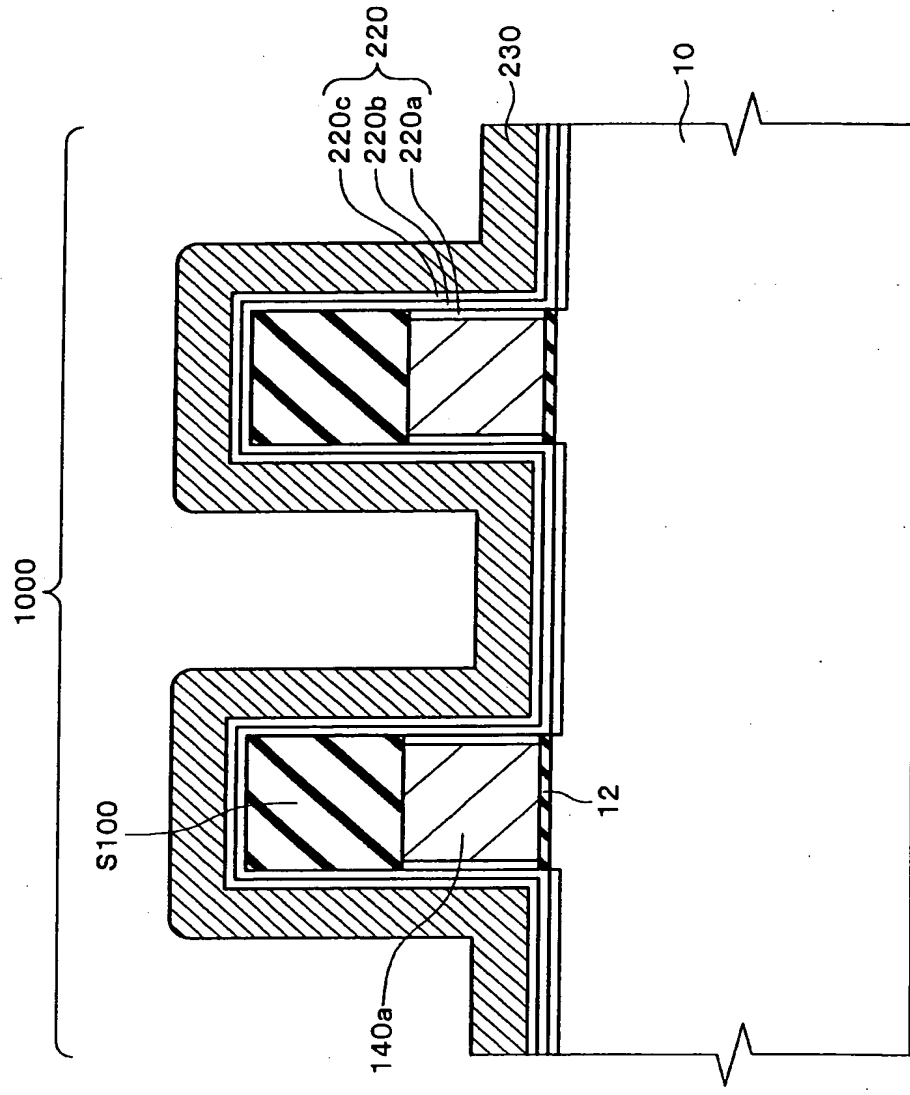


FIG. 9

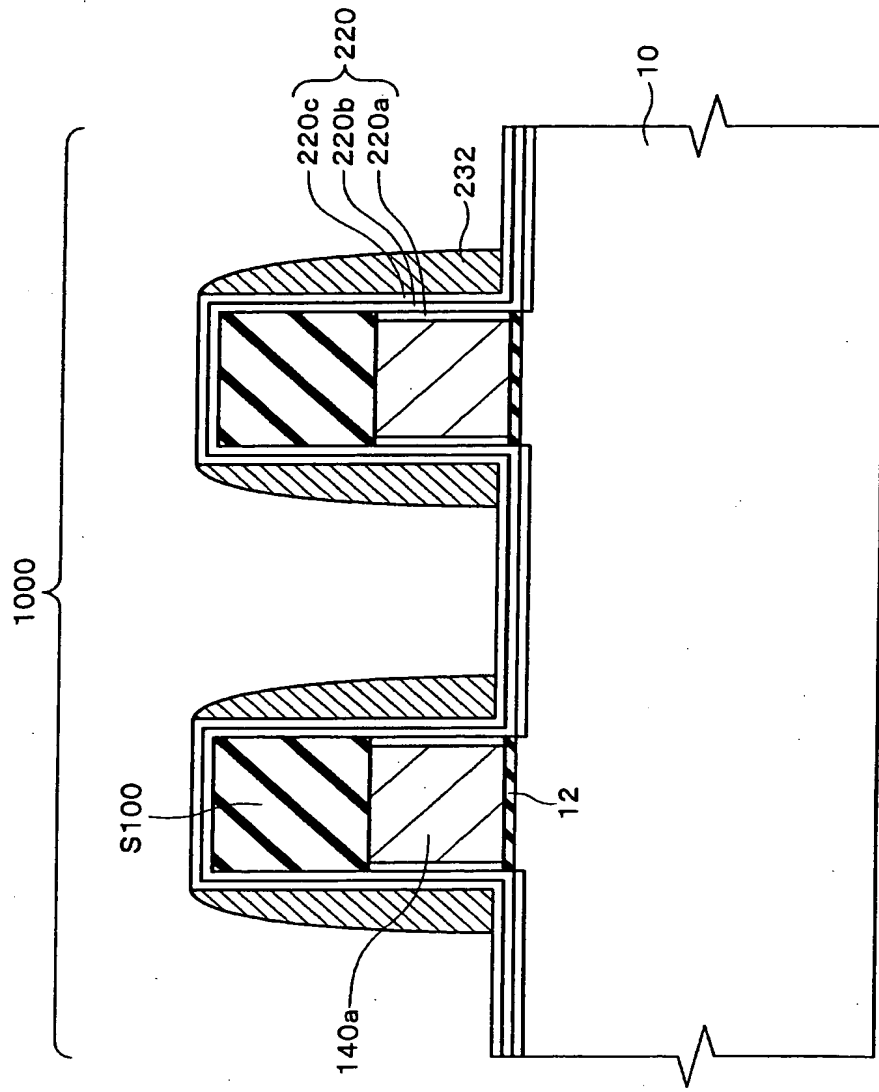


FIG. 10

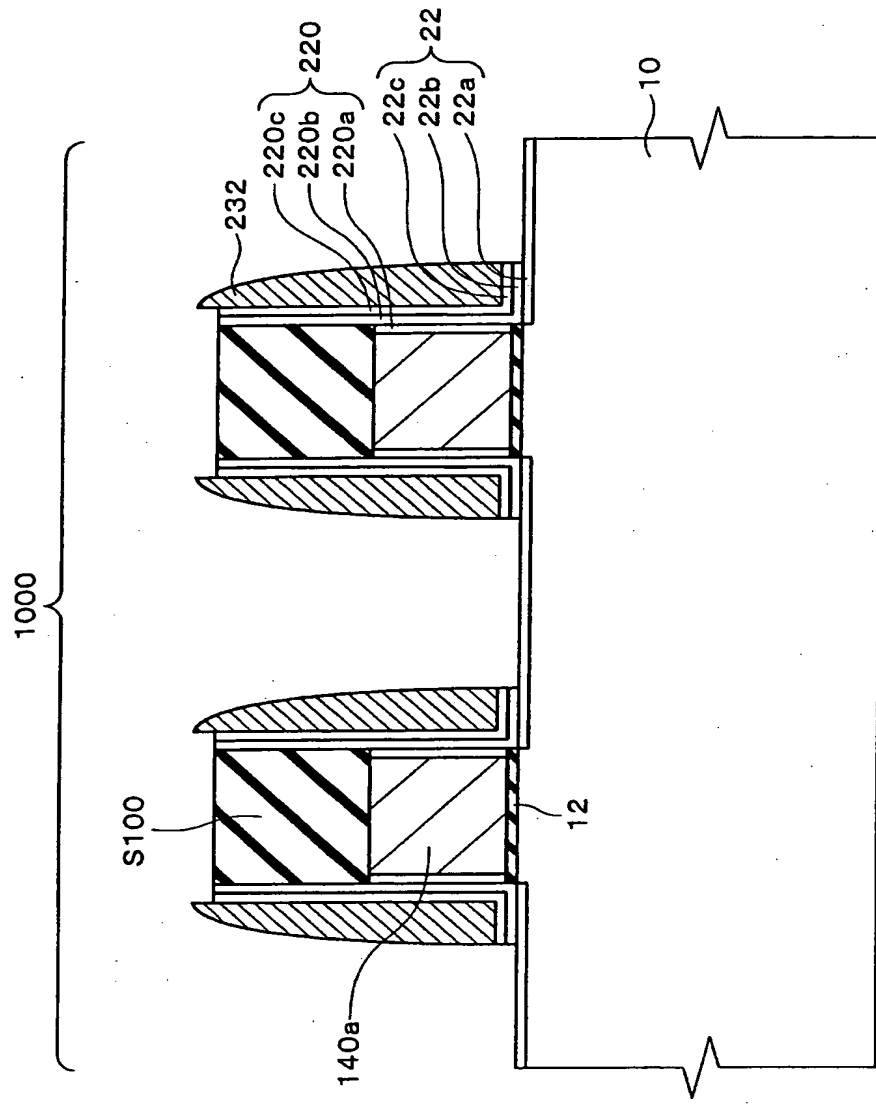


FIG. 11

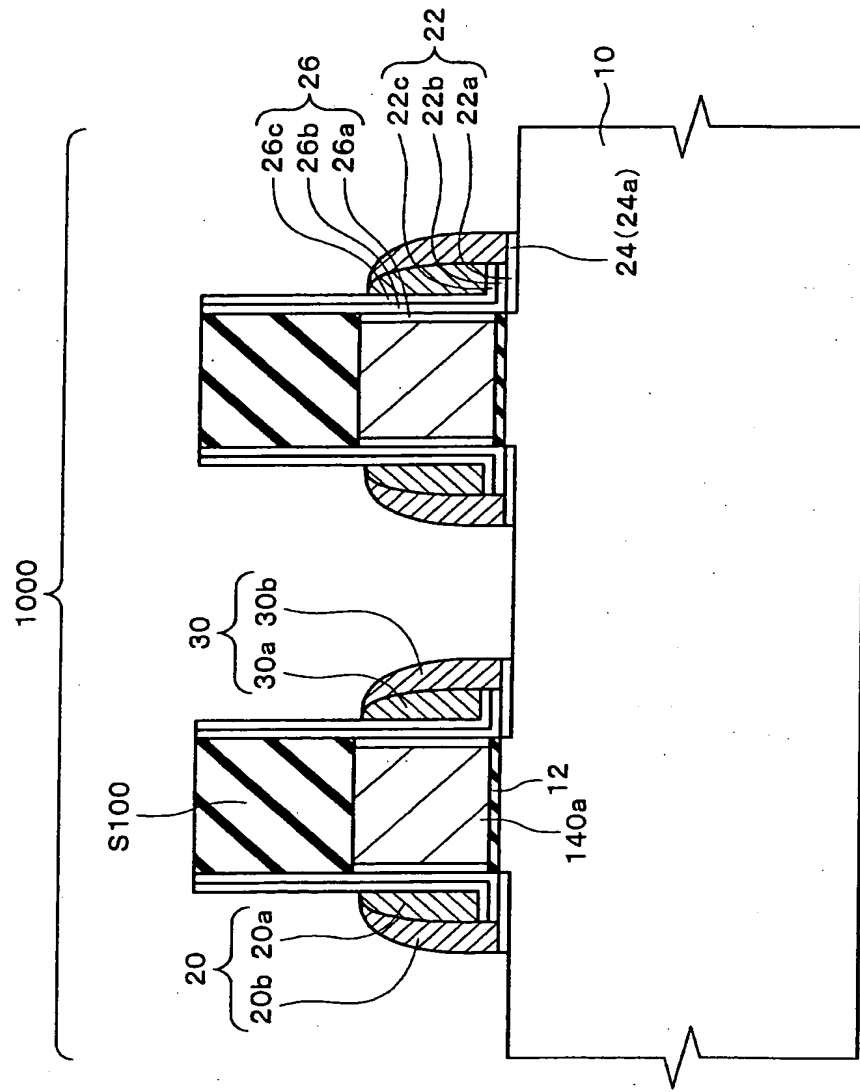


FIG. 12

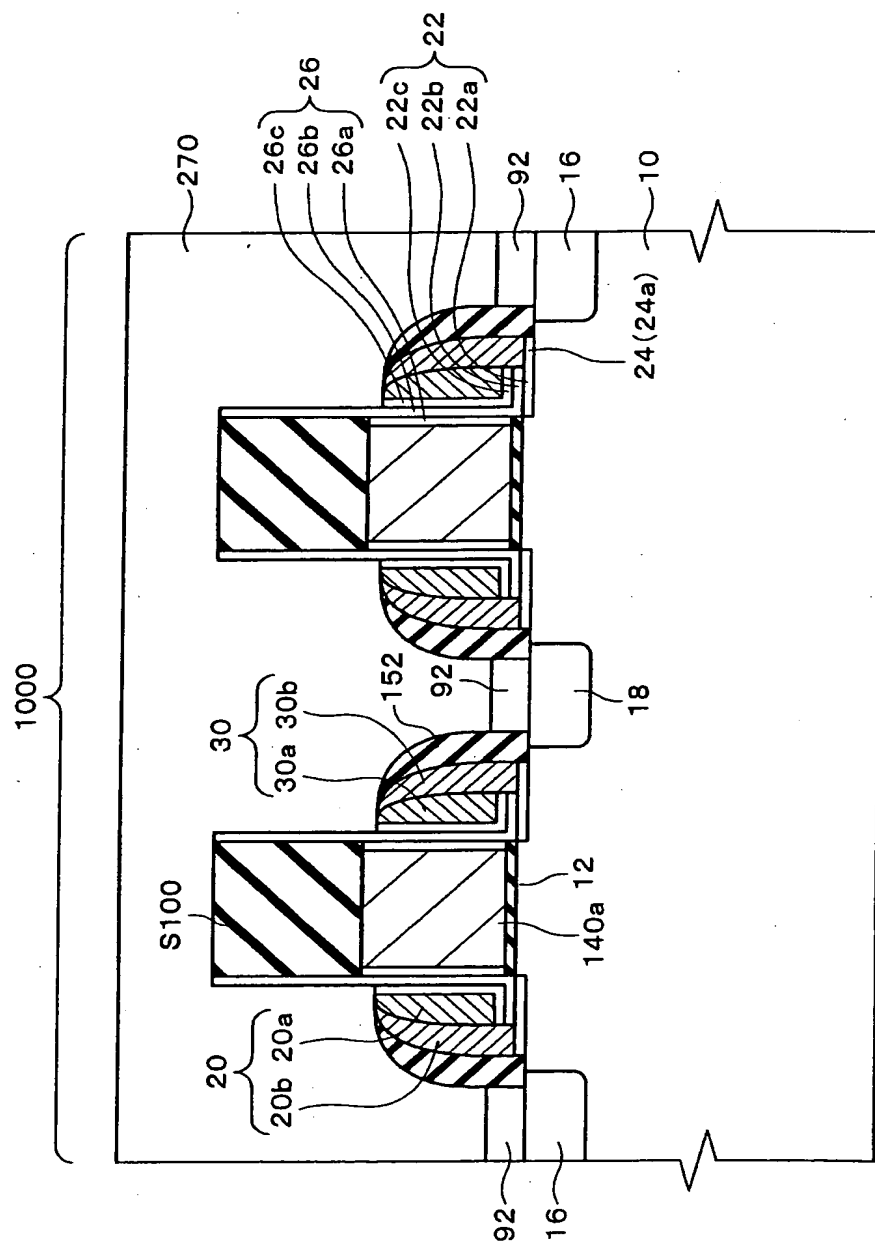


FIG. 13

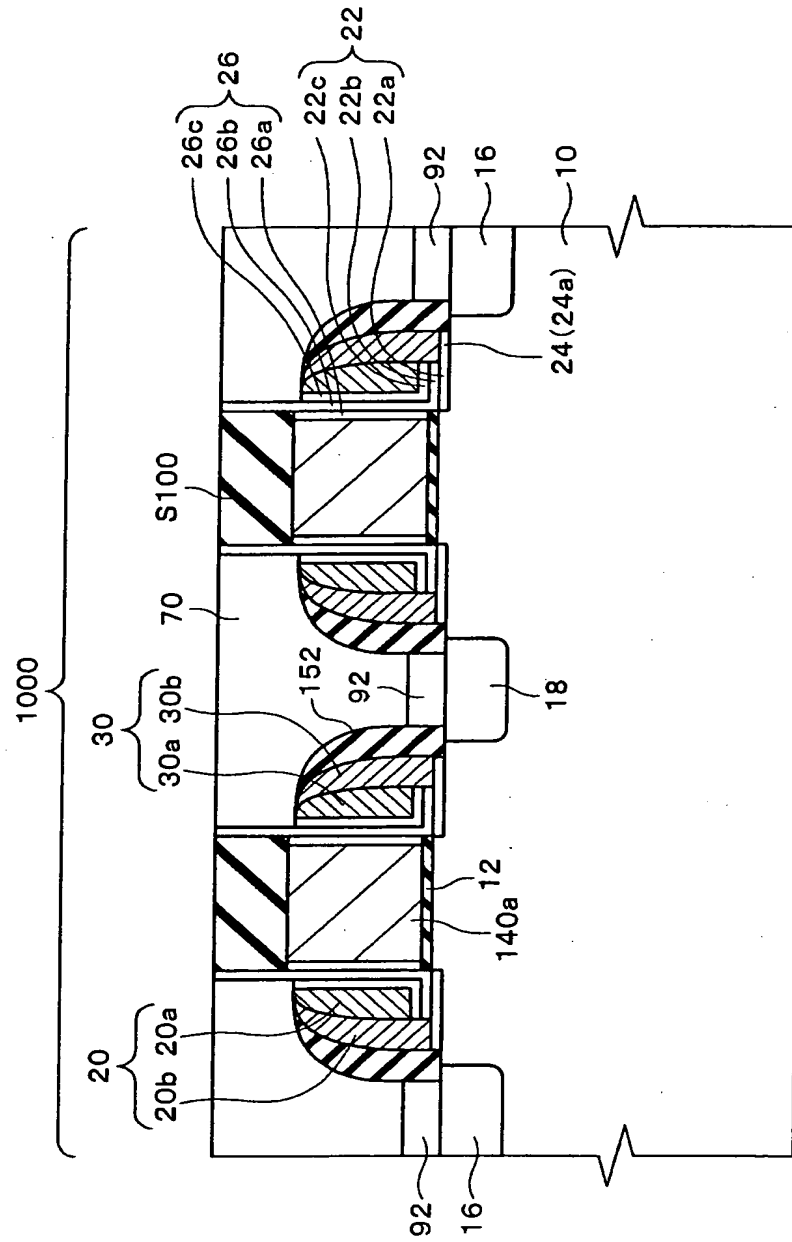


FIG. 14

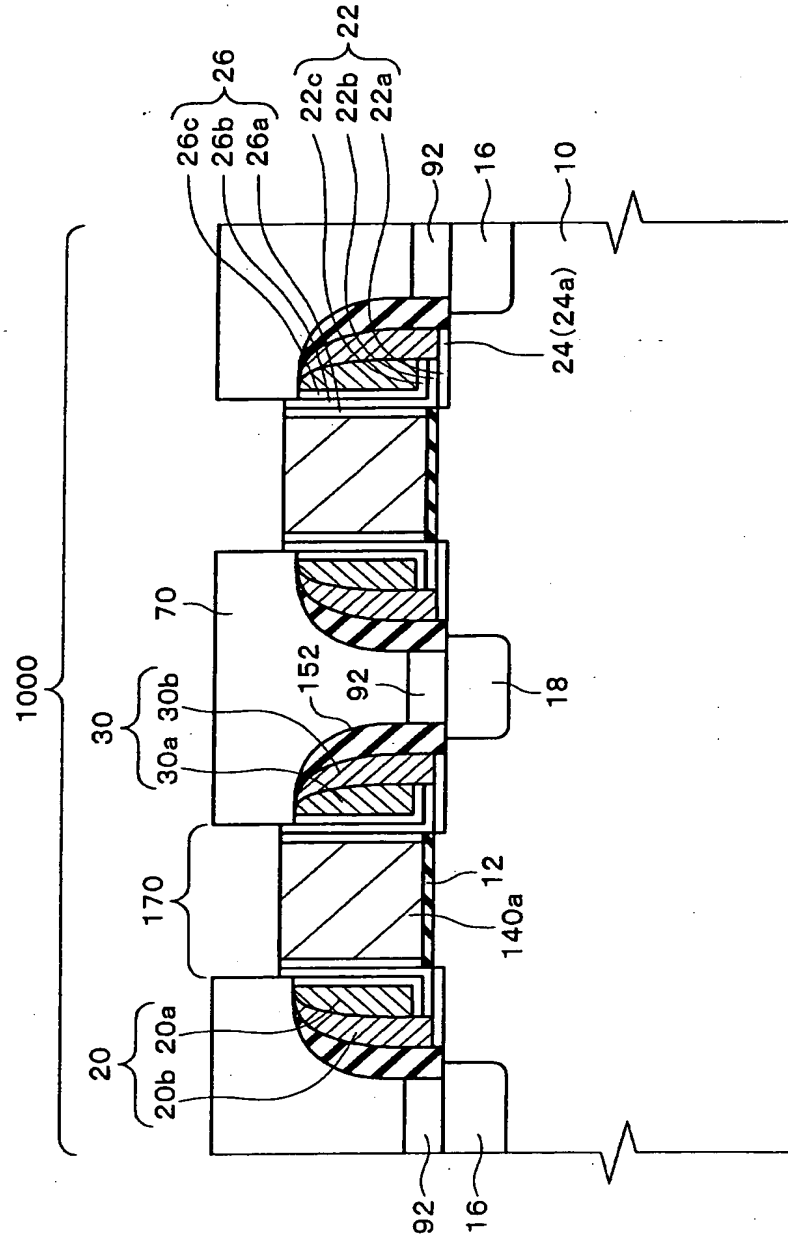


FIG. 15

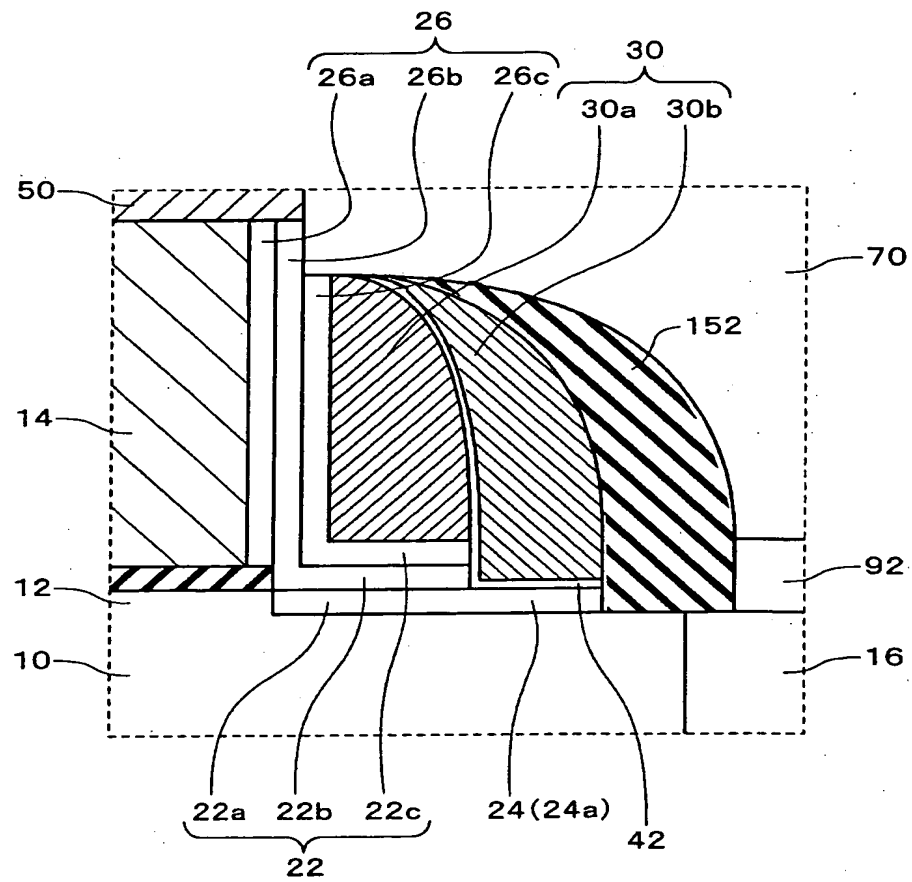
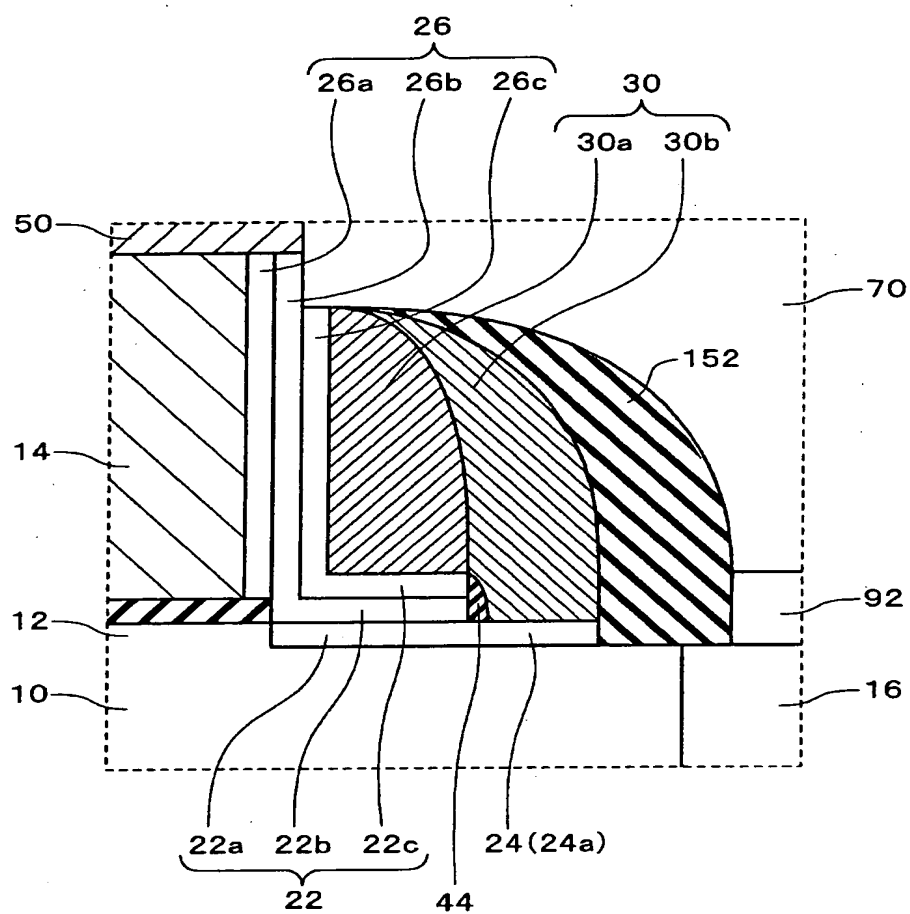


FIG. 16



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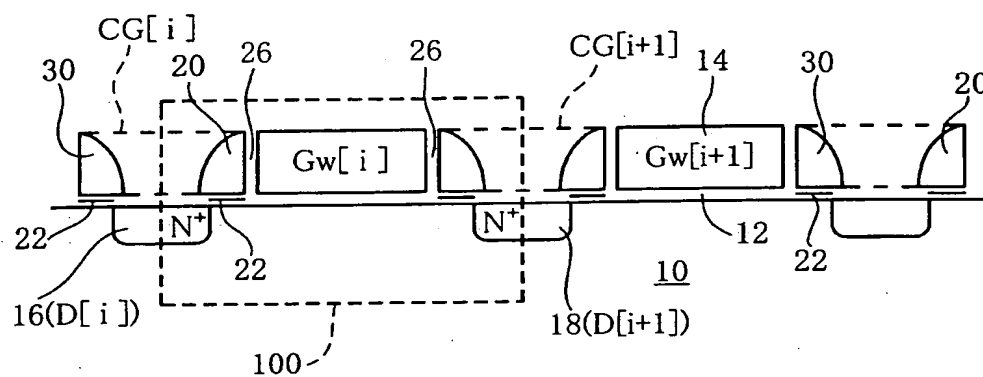


FIG. 18

